In the claims:

Please cancel claims 1, 2, 5 and amend claims 3, 6, 7, 8, 11 as follows:

1. (canceled)

2. (canceled)

3. (currently amended) A Peripheral Component Interconnect (PCI) bridge comprising:

a first interface to a first PCI bus;

a second interface to a second PCI bus;

a cache buffer for storing data read from a PCI-bus memory for a current command;

prefetch control means for fetching data from the PCI-bus memory into the cache buffer for the current command, the prefetch control means fetching a maximum amount of data determined by a prefetch count;

wherein the current command is a read command or a read-multiple command, the read-multiple command able to read a larger amount of data than the read command;

first statistical means, responsive when the current command is the read command to read from the PCI-bus memory on the first PCI bus, for generating the prefetch count for the read command by storing statistics indicating under-fetching and over-fetching of prior read commands; and

second statistical means, responsive when the current command is the read-multiple command to read from the PCI-bus memory on the first PCI bus, for generating the prefetch count for the read-multiple command by storing statistics indicating under-fetching and over-fetching of prior read-multiple commands;

wherein the first statistical means further comprises:

first prefetch count means for generating the prefetch count when the current command is the read command;

first under-prefetching count means for tracking read commands wherein the prefetch control means under-prefetched data into the cache buffer;

first over-prefetching count means for tracking read commands wherein the prefetch control means over-prefetched data into the cache buffer;

first adjust means, coupled to the first prefetch count means, for increasing the prefetch count generated by the first prefetch count means in response to the first under-prefetching count means indicating that insufficient data was prefetched into the cache buffer in the prior read commands, and for decreasing the prefetch count generated by the first prefetch count means in response to the first over-prefetching count means indicating that un-read data was prefetched into the cache buffer in the prior read commands;

wherein the second statistical means further comprises:

second prefetch count means for generating the prefetch count when the current command is the read-multiple command;

second under-prefetching count means for tracking read-multiple commands wherein the prefetch control means under-prefetched data into the cache buffer;

second over-prefetching count means for tracking read-multiple commands wherein the prefetch control means over-prefetched data into the cache buffer; and

second adjust means, coupled to the second prefetch count means, for increasing the prefetch count generated by the second prefetch count means in response to the second under-prefetching count means indicating that insufficient data was prefetched into the cache buffer in the prior read-multiple commands, and for decreasing the prefetch count generated by the second prefetch count means in response to the second over-prefetching count means indicating that un-read data was prefetched into the cache buffer in the prior read-multiple commands;

~~The PCI bridge of claim 2~~ wherein the first under-prefetching means comprises a first disconnect means for advancing an indication of under-prefetching when the read command is terminated by the PCI-bus memory disconnecting from the first PCI bus before sufficient data is transferred to the cache buffer;

wherein the first over-prefetching means comprises a first discard means for advancing an indication of over-prefetching when the read command terminates before all data prefetched from the PCI-bus memory for the read command is read by a requestor that generated the read command;

wherein the second under-prefetching means comprises a second disconnect means for advancing an indication of under-prefetching when the read-multiple command is terminated by the PCI-bus memory disconnecting from the second PCI bus before sufficient data is transferred to the cache buffer;

wherein the second over-prefetching means comprises a second discard means for advancing an indication of over-prefetching when the read-multiple command terminates before all data prefetched from the PCI-bus memory for the read-multiple command is read by a requestor that generated the read-multiple command,

whereby separate prefetching statistics for the read command and for the read-multiple command generate the prefetch count.

4. (original) The PCI bridge of claim 3 wherein the first statistical means further comprises:

first completion means for counting a number of the prior read commands that completed;

first reset means, coupled to the first adjust means, for resetting the first completion means, the first under-prefetching means, and the first over-prefetching means after a predetermined number of the prior read commands have completed;

wherein the second statistical means further comprises:

second completion means for counting a number of the prior read-multiple commands that completed; and

second reset means, coupled to the second adjust means, for resetting the second completion means, the second under-prefetching means, and the second over-prefetching means after a predetermined number of the prior read-multiple commands have completed.

5. (canceled)

6. (currently amended) A Peripheral Component Interconnect (PCI) bridge comprising:

a first interface to a first PCI bus;

a second interface to a second PCI bus;

a cache buffer for storing data read from a PCI-bus memory for a current command;

prefetch control means for fetching data from the PCI-bus memory into the cache buffer for the current command, the prefetch control means fetching a maximum amount of data determined by a prefetch count;

wherein the current command is a read command or a read-multiple command, the read-multiple command able to read a larger amount of data than the read command;

first statistical means, responsive when the current command is the read command to read from the PCI-bus memory on the first PCI bus, for generating the prefetch count for the read command by storing statistics indicating under-fetching and over-fetching of prior read commands; and

second statistical means, responsive when the current command is the read-multiple command to read from the PCI-bus memory on the first PCI bus, for generating the prefetch count for the read-multiple command by storing statistics indicating under-fetching and over-fetching of prior read-multiple commands;

wherein the current command is a read-line command that is able to read less data than the read-multiple command, and able to read a larger amount of data than the read command;

third statistical means, responsive when the current command is the read-line command to read from the PCI-bus memory on the first PCI bus, for generating the prefetch count for the read-line command by storing statistics indicating under-fetching and over-fetching of prior read-line commands;

~~The PCI bridge of claim 5~~ wherein the third statistical means further comprises:

third prefetch count means for generating the prefetch count when the current command is the read-line command;

third under-prefetching count means for tracking read-line commands wherein the prefetch control means under-prefetched data into the cache buffer;

third over-prefetching count means for tracking read-line commands wherein the prefetch control means over-prefetched data into the cache buffer;

third adjust means, coupled to the third prefetch count means, for increasing the prefetch count generated by the third prefetch count means in response to the third under-prefetching count means indicating that insufficient data was prefetched into the cache buffer in the prior read-line commands, and for decreasing the prefetch count generated by the third prefetch count means in response to the third over-prefetching count means indicating that un-read data was prefetched into the cache buffer in the prior read-line commands;

third completion means for counting a number of the prior read-line commands that completed; and

third reset means, coupled to the third adjust means, for resetting the third completion means, the third under-prefetching means, and the third over-prefetching means after a predetermined number of the prior read-line commands have completed, whereby separate prefetching statistics for the read command and for the read-multiple command generate the prefetch count.

7. (currently amended) The PCI bridge of claim 6 wherein the read-line command reads an amount of data ranging from a portion of one line in the cache buffer, up to two lines ~~substantially equal to a line~~ in the cache buffer.

8. (currently amended) A Peripheral Component Interconnect (PCI) bridge comprising:

a first interface to a first PCI bus;

a second interface to a second PCI bus;

a cache buffer for storing data read from a PCI-bus memory for a current command;

prefetch control means for fetching data from the PCI-bus memory into the cache buffer for the current command, the prefetch control means fetching a maximum amount of data determined by a prefetch count;

wherein the current command is a read command or a read-multiple command, the read-multiple command able to read a larger amount of data than the read command;

first statistical means, responsive when the current command is the read command to read from the PCI-bus memory on the first PCI bus, for generating the prefetch count

for the read command by storing statistics indicating under-fetching and over-fetching of prior read commands;

second statistical means, responsive when the current command is the read-multiple command to read from the PCI-bus memory on the first PCI bus, for generating the prefetch count for the read-multiple command by storing statistics indicating under-fetching and over-fetching of prior read-multiple commands;

~~The PCI bridge of claim 1~~ wherein the current command is the read command, ~~the~~ a read-line command, or the read-multiple command to read from the second PCI bus or from the first PCI bus;

first reverse statistical means, responsive when the current command is the read command to read from the PCI-bus memory on the second PCI bus, for generating the prefetch count for the read command by storing statistics indicating under-fetching and over-fetching of prior read commands; ~~and~~

second reverse statistical means, responsive when the current command is the read-multiple command to read from the PCI-bus memory on the second PCI bus, for generating the prefetch count for the read-multiple command by storing statistics indicating under-fetching and over-fetching of prior read-multiple commands; and

third reverse statistical means, responsive when the current command is the read-line command to read from the PCI-bus memory on the second PCI bus, for generating the prefetch count for the read-line command by storing statistics indicating under-fetching and over-fetching of prior read-line commands,

whereby separate prefetching statistics for the read command and for the read-multiple command generate the prefetch count and whereby separate prefetching statistics are used when the PCI-bus memory is on the second PCI bus and when on the first PCI bus.

9. (original) The PCI bridge of claim 8 wherein the second reverse statistical means further comprises:

second reverse prefetch count means for generating the prefetch count when the current command is the read-multiple command;

second reverse under-prefetching count means for tracking read-multiple commands wherein the prefetch control means under-prefetched data into the cache buffer;

second reverse over-prefetching count means for tracking read-multiple commands wherein the prefetch control means over-prefetched data into the cache buffer;

second reverse adjust means, coupled to the second reverse prefetch count means, for increasing the prefetch count generated by the second reverse prefetch count means in response to the second reverse under-prefetching count means indicating that insufficient data was prefetched into the cache buffer in the prior read-multiple commands, and for decreasing the prefetch count generated by the second reverse prefetch count means in response to the second reverse over-prefetching count means indicating that un-read data was prefetched into the cache buffer in the prior read-multiple commands;

second reverse completion means for counting a number of the prior read-multiple commands that completed;

second reverse reset means, coupled to the second reverse adjust means, for resetting the second reverse completion means, the second reverse under-prefetching means, and the second reverse over-prefetching means after a predetermined number of the prior read-multiple commands have completed.

10. (original) The PCI bridge of claim 9 wherein the third reverse statistical means further comprises:

third reverse prefetch count means for generating the prefetch count when the current command is the read-line command;

third reverse under-prefetching count means for tracking read-line commands wherein the prefetch control means under-prefetched data into the cache buffer;

third reverse over-prefetching count means for tracking read-line commands wherein the prefetch control means over-prefetched data into the cache buffer;

third reverse adjust means, coupled to the third reverse prefetch count means, for increasing the prefetch count generated by the third reverse prefetch count means in response to the third reverse under-prefetching count means indicating that insufficient data was prefetched into the cache buffer in the prior read-line commands, and for decreasing the prefetch count generated by the third reverse prefetch count means in response to the third reverse over-prefetching count

means indicating that un-read data was prefetched into the cache buffer in the prior read-line commands;

third reverse completion means for counting a number of the prior read-line commands that completed;

third reverse reset means, coupled to the third reverse adjust means, for resetting the third reverse completion means, the third reverse under-prefetching means, and the third reverse over-prefetching means after a predetermined number of the prior read-line commands have completed.

11. (currently amended) A prefetching predictor for predicting prefetching of data from a bus to a cache comprising:

a first set of counters for predicting a first length of data to prefetch for a first read command;

a second set of counters for predicting a second length of data to prefetch for a second read command;

a third set of counters for predicting a third length of data to prefetch for a third read command;

each of the first, second, and third set of counters comprising:

a prefetch-length counter that indicates a data length to prefetch;

a disconnect counter that is advanced for each matching command that is disconnected by a bus slave; and

a discard counter that is advanced for each matching command ~~that is discards~~ that discards prefetched data in the cache;

wherein a matching command is the first read command for the first set of counters, the second read command for the second set of counters, or the third read command for the third set of counters;

wherein the first read command, the second read command, and the third read command are commands for reading differing amounts of data from the bus slave,

whereby sets of counters are kept for read commands for differing amounts of data.

12. (original) The prefetching predictor of claim 11 wherein the matching command is sent by a bus master requesting to read from the bus slave, the discard counter in a matching set of counters being advanced when the bus master terminates reading and prefetched data in the cache is discarded.

13. (original) The prefetching predictor of claim 11 further comprising:

a data fetcher for reading data from the bus slave on the bus in response to the first, second, or third read command, the data fetcher attempting to read an amount of data from the bus slave indicated by the prefetch-length counter in the first set of counters in response to the first read command, or the prefetch-length counter in the second set of counters in response to the second read command, or the prefetch-length counter in the third set of counters in response to the third read command.

14. (original) The prefetching predictor of claim 13:

wherein the first read command has a first data length of one to eight bytes;

wherein the second read command has a second data length of one cache line;

wherein the third read command has a third data length of more than one cache line;

wherein the one cache line is at least 128 bytes.

15. (original) The prefetching predictor of claim 13 wherein the first read command is a read-memory (MR) command;

wherein the second read command is a read-memory-line (MRL) command;

wherein the third read command is a read-memory-multiple (MRM) command.

16. (original) The prefetching predictor of claim 13 wherein each of the first, second, and third set of counters further comprises:

a completion counter that is advanced for each completed command of a matching command type.

17. (original) The prefetching predictor of claim 16 further comprising:

a prefetch adjustor, activated to adjust the prefetch-length counter in a selected set of counters when the completion counter in the selected set of counters reaches a pre-determined number, the prefetch adjustor decrementing the prefetch-length counter when the discard counter reaches a discard-count value, the prefetch adjustor incrementing the prefetch-length counter when the disconnect counter reaches a disconnect-count value;

wherein the selected set is the first, second, or third set of counters.

18. (original) The prefetching predictor of claim 17 further comprising:

counter reset logic, activated by the prefetch adjustor, the counter reset logic clearing the discard counter, the disconnect counter, and the completion counter in the selected set of counters after the completion counter in the selected set of counters reaches the pre-determined number.

19. (original) A prefetch-length prediction method comprising:

receiving a read command from a bus master, the read command being a read command, or a read-multiple command, the read-multiple command being able to read more data from a bus slave than the read command;

incrementing a read-completion counter upon completion of the read command;

incrementing a read-discard counter when the read command is terminated by the bus master and prefetched data for the read command in a cache is discarded;

incrementing a read-disconnect counter when the read command is terminated by the bus slave before the bus master finishes reading data and no prefetched data for the read command in the cache is discarded;

incrementing a read-multiple-completion counter upon completion of the read-multiple command;

incrementing a read-multiple-discard counter when the read-multiple command is terminated by the bus master and prefetched data for the read-multiple command in a cache is discarded;

incrementing a read-multiple-disconnect counter when the read-multiple command is terminated by the bus slave before the bus master finishes reading data and no prefetched data for the read-multiple command in the cache is discarded;

when the read-completion counter reaches a predetermined count, incrementing a read-prefetch counter when the read-disconnect counter exceeds a disconnect threshold, decrementing the read-prefetch counter when the read-discard counter exceeds a discard threshold, and clearing the read-completion counter, the read-discard counter, and the read-disconnect counter;

when the read-multiple-completion counter reaches a predetermined count, incrementing a read-multiple-prefetch counter when the read-multiple-disconnect counter exceeds the disconnect threshold, decrementing the read-multiple-prefetch counter when the read-multiple-discard counter exceeds the discard threshold, and clearing the read-multiple-completion counter, the read-multiple-discard counter, and the read-multiple-disconnect counter;

prefetching up to a number of cache lines indicated by the read-prefetch counter when the read command is executed; and

prefetching up to a number of cache lines indicated by the read-multiple-prefetch counter when the read-multiple command is executed,

whereby prefetch length is separately predicted for the read command and the read-multiple command.

20. (original) The prefetch-length prediction method of claim 19 wherein the read command is a read-line command, the read command, or the read-multiple command, the read-line command being able to read more data from a bus slave than the read command, the read-multiple command being able to read more data from a bus slave than the read-line command or the read command;

further comprising:

incrementing a read-line-completion counter upon completion of the read-line command;

incrementing a read-line-discard counter when the read-line command is terminated by the bus master and prefetched data for the read-line command in a cache is discarded;

incrementing a read-line-disconnect counter when the read-line command is terminated by the bus slave before the bus master finishes reading data and no prefetched data for the read-line command in the cache is discarded;

when the read-line-completion counter reaches a predetermined count, incrementing a read-line-prefetch counter when the read-line-disconnect counter exceeds the disconnect threshold, decrementing the read-line-prefetch counter when the read-line-discard counter exceeds the discard threshold, and clearing the read-line-completion counter, the read-line-discard counter, and the read-line-disconnect counter; and

prefetching up to a number of cache lines indicated by the read-line-prefetch counter when the read-line command is executed.